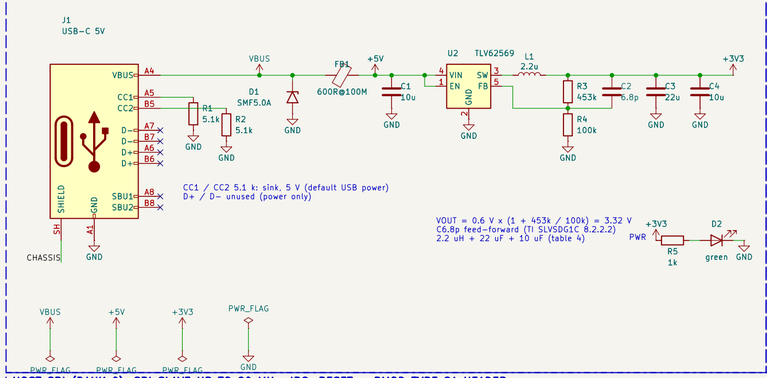
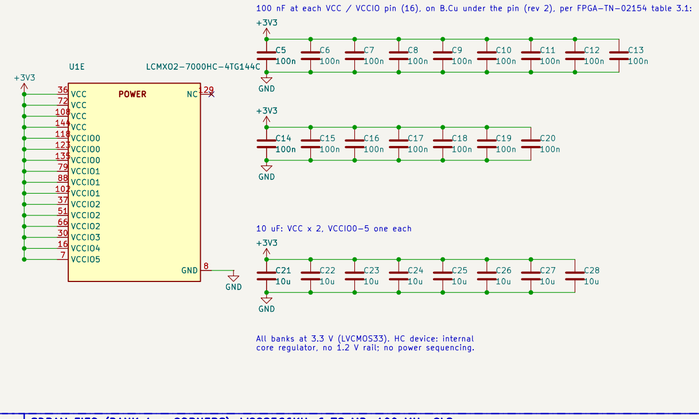
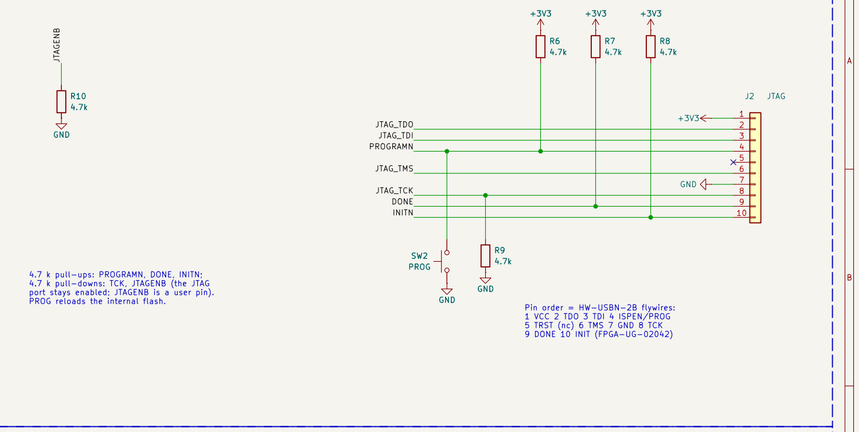
POWER INPUT: USB-C 5 V, TVS, FERRITE, TLV62569 BUCK 3.3 V / 2 A



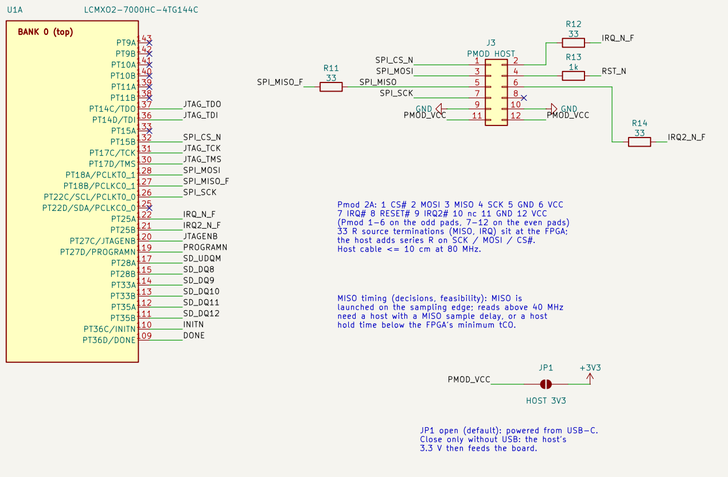
FPGA POWER: VCC + VCCIO0–5 FROM 3.3 V, 100 nF AT EVERY PIN, 10 uF PER BANK



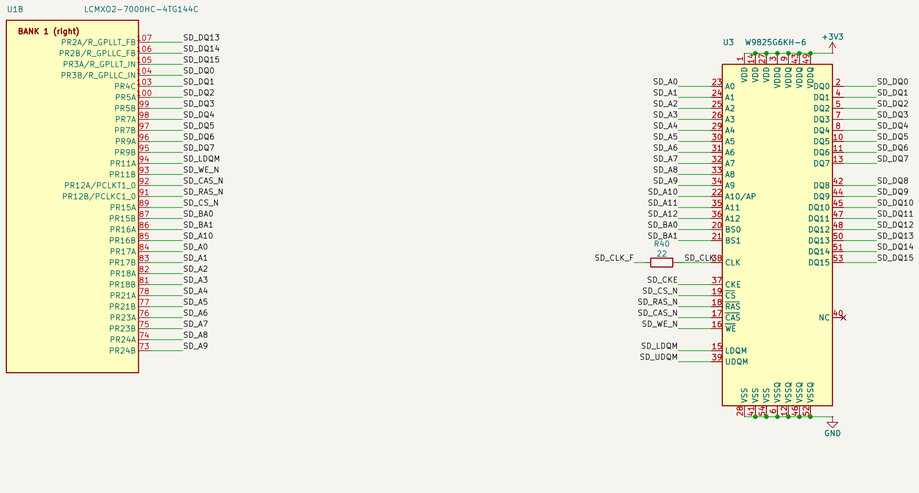
CONFIGURATION + JTAG (internal flash; Lattice HW-USBN-2B, 1 x 10)



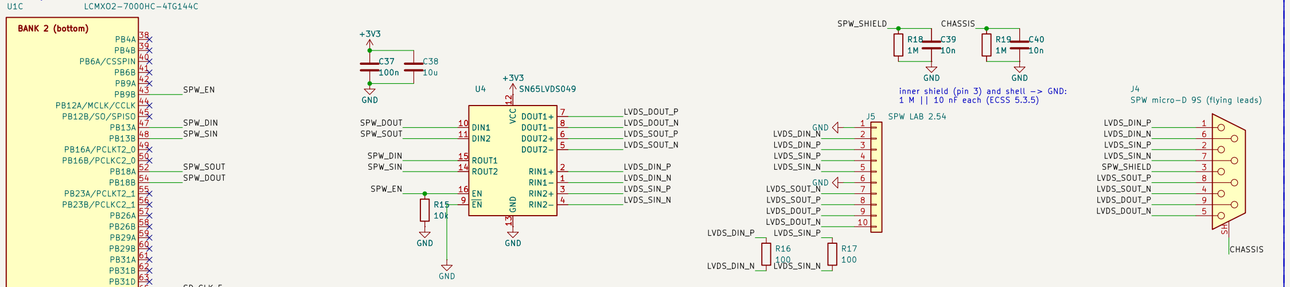
HOST SPI (BANK 0): SPI SLAVE UP TO 80 MHz, IRQ, RESET — PMOD TYPE 2A HEADER



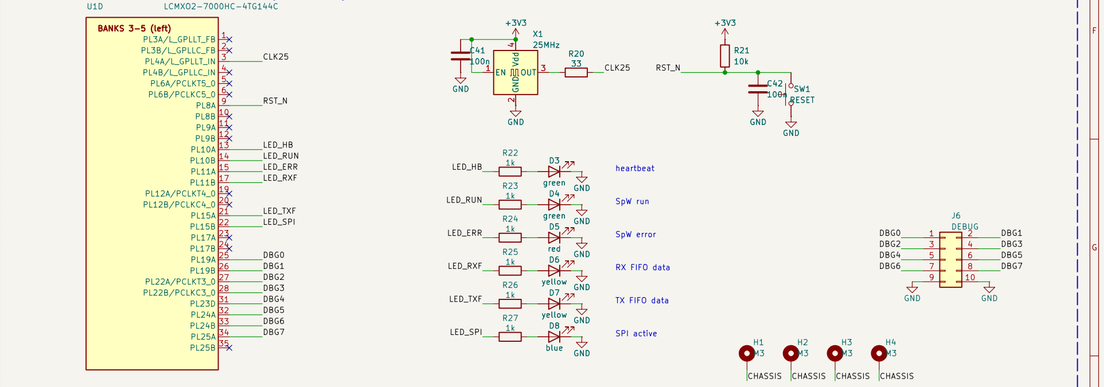
SDRAM FIFO (BANK 1 + CORNERS): W9825G6KH-6 32 MB, 100 MHz CL2



SPACEWIRE (BANK 2): SN65LVDS049, MICRO-D RECEPTACLE OR 2.54 mm LAB HEADER



CLOCK, RESET, STATUS LEDS, DEBUG HEADER (BANKS 3–5)



USB-C 5 V -> TLV62569 3.3 V (one rail); JTAG 1 x 10 for HW-USBN-2B
SPI slave to 80 MHz (Pmod 2A) + IRQ; SpaceWire 100 Mbit/s
MachXO2-7000HC, W9825G6KH 32 MB SDRAM FIFO, SN65LVDS049 PHY

Sheet: /
File: spacewire_spi_bridge.kicad_sch

Title: SpaceWire to SPI bridge with SDRAM FIFO

Size: A2	Date: 2026-11-03	Rev: 2
KiCad E.D.A. 10.0.4		Id: 1/1